Remarks

This is a complete response to the pending Office Action mailed 10/25/2005. At the outset, Applicant expresses appreciation for the Examiner's responses to Applicant's previous arguments.

In response, these remarks are proper and do not add new matter, but more particularly point out and distinctly claim that which is the patentable subject matter in order to clarify Applicant's position that all claims are in condition for allowance.

Applicant has made corrections to the specification herein to correct typographical mistakes.

This is a request for the Examiner to reconsider and withdraw the final rejection of all pending claims. Absent such reconsideration, this case is not in condition for appeal due to unresolved issues making all rejections of independent claims not proper and without basis. Following is an explanation of at least some of the unresolved issues discussed below.

The examination resulting in the anticipatory rejection of claims 1 and 16 is incomplete because it is based on the mischaracterization that Liu '617 updates the registers 320 over the host bus 215. Absent the mischaracterization, the cited reference does not identically disclose all the features of the rejected claim. Thus, the Examiner has not substantiated a prima facie case of anticipation.

The examination resulting in the anticipatory rejection of claims 6 and 15 is incomplete because it is based on the mischaracterization that Liu '617 discloses the RAM 222 being a memory table with values indexed by a zone identifier. Absent the mischaracterization, the cited reference does not identically disclose all the features of the

rejected claim. Thus, the Examiner has not substantiated a prima facie case of anticipation.

Rejection Under Section 102(b)

Claims 1 and 16-19 were again rejected as being anticipated by Liu '617. Applicant respectfully reiterates its earlier traversal of this rejection. (see Applicant's response of 8/10/2005)

Claim 1

The Examiner has not substantiated the requisite prima facie case of anticipation because Liu '617 does not identically disclose all the features of the present embodiments according to claim 1, which include at least the following:

> *a method...comprising steps of: (a) retrieving a first portion of the recorded data via the bus; (b) updating some of the registers via the bus; and (c) retrieving a second portion of the recorded data via the bus.*
> (excerpt of claim 1, emphasis added)

Applicant previously argued that Liu '617 clearly does not disclose *updating some of the register via the bus* as in the present embodiments as claimed:

> Liu further discloses that automatic read sequencer 250 and automatic write sequencer 260 automatically "update" the head number, cylinder address, sector address and the number of sectors to be transferred in the task file registers of computer bus interface circuit 234. The update function disclosed in Liu is not done via the bus 215. Therefore, that disclosure does not identically show updating at least one register or parameter via the bus....
> (Applicant's response of 8/10/2005, pg. 6, emphasis added)

The Examiner maintained the anticipatory rejection by relying on the same passages of Liu '617 as in the previous rejection. However, the skilled artisan recognizes

that even the passage of Liu '617 on which the Examiner relies clearly distinguishes the difference between how the host 210 and the bus interface circuit 234 interact with the registers 320. Particularly, clearly the host 210 sets the registers 320 while the bus interface circuit 234 updates the registers 320:

> In addition to eliminating performance degradations associated with host computer interrupt processing, host computer 210 initially sets the head number, cylinder address, sector address, and the number of sectors to be transferred in task file registers of computer bus interface circuit 234. After a sector of data has been transferred to host computer 210, automatic read sequencer 250 of this invention automatically updates the head number, cylinder address, sector address, and the number of sectors remaining to be transferred in task file registers of computer bus interface circuit 234. In contrast, prior art systems required microprocessor 121 (FIG. 1) to individually update each of the task file registers. Consequently, the processing overhead for microprocessor 221 is reduced in comparison to that of microprocessor 121...As explained more completely below, the operation of automatic write sequencer 260 is similar to that of automatic read sequencer 250 except that multiple sectors of data are transferred from data bus 215 to RAM 222 without intervention by microprocessor 221. Initially, host computer 210 sets the head number, cylinder address, sector address, and the number of sectors to be transferred in task file registers of computer bus interface circuit 234. After a sector of data has been transferred from host computer 210, automatic write sequencer 260 automatically updates the cylinder address, sector address, and the number of sectors remaining to be transferred in task file registers of computer bus interface circuit 234.
>
> (Liu '617 col. 8 line 28 to col. 9 line 2, emphasis added)

Liu '617 employs use of the term "update," or some form thereof, at least 40 times. Not once is "update" used to describe anything other than the bus interface circuit 234 responding to a data transfer command, after the data transfer command was initiated by the host 210. More particularly, not once is the term "update" used in describing the

function of the host 210 when it writes information to the registers 320 in relation to a data transfer command (read or write). Rather, "updating" in Liu '617 is always defined in relation to transient state information between the bus interface circuit 234 and the registers 320 that is not passed over the host bus 215. Some passages that illustrate this explicitly defined meaning in Liu '617 are:

> The computer bus interface circuit of this invention not only automatically transfers data between the computer data bus and the computer bus interface circuit but also generates status information, generates interrupts to the host computer, and updates task file registers.
> (Liu '617, Abstract, emphasis added)

> The automatic read sequencer of this invention employs a novel process to automatically transfer data from the disk drive to the host computer. In this process, the automatic read sequencer first decrements the value of the number of sectors to be transferred in response to the read sector command from the host computer. Next, the status of the disk drive is updated and data is prefetched from a buffer control memory to a memory of the automatic read sequencer. When the automatic read sequencer memory is nearly full, an interrupt is sent to the host computer telling the computer that the data is ready for transfer from the automatic read sequencer.
> (Liu '617, col. 4 lines 17-28, emphasis added)

> In response to the signal on line HPEN, auto-read control circuit 350 decrements sector counter 330, i.e., performs step 402, update sector counter. Thus, automatic read sequencer 250 automatically updates this portion of the task file, according to the principles of this invention.
> (Liu '617, col. 11 lines 1-5, emphasis added)

Accordingly, the skilled artisan readily understands that Liu '617 discloses setting the registers 320 with the host 210 over the host bus 215 commensurate with a data transfer command, and subsequently updating the registers 320 with the bus interface circuit 234 not over the host bus 215 until the data transfer command is completed.

However, the Examiner must mischaracterize Liu '617 as disclosing the host "updating the registers" in order to make an argument that the "updating" occurs over the host bus 215:

> Liu teaches every read operation start with the host writing values to a set of registers (see lines 28-42 of column 8). Therefor, after an initial read operation has completed, the next time the host desires to read a different portion of data, stored at a different location, the host will update the registers with values pertaining to the subsequent read operation.
> (Office Action of 10/25/2005, pg. 13)

There clearly is no support from Liu '617 for the Examiner's argument that the host 210 updates the registers 320. The skilled artisan recognizes that "writing to the registers" and "updating the registers" mean entirely different things. That is, the host 210 "writes" values to the registers associated with information such as the location and size of the data transfer. The bus interface circuit 234 "updates" the values that were previously "written" in order to monitor and control the transient state of the data transfer to completion. Generally, each data transfer command will be associated with one "writing" to the registers and a plurality of transient "updating" of the registers until the data transfer command is either completed or otherwise aborted.

The Examiner's mischaracterization is not just tenuous, but is directly contrary to the disclosure of Liu '617. First, Liu '617 purposefully does not update the registers 320 over the host bus 215 in order to offload the processing overhead associated with the updating functions. (see, for example, Liu '617 col. 5 lines 17-23) Also, the transient updating of the registers 320 in Liu '617 is eventually completed when the associated data transfer command is completed or aborted. Liu '617 explicitly does not disclose,

and the skilled artisan readily understands the futility of suggesting an updating of registers in this context beyond completion of the associated data transfer command.

Thus, this meaning of the claim phrase *updating some of the registers via the bus* as defined by Liu '617, and the meaning ascribed thereto by the skilled artisan, is consistent with its meaning as used in the present specification. For illustrative purposes, FIG. 3 and the description thereof show how in the present embodiments as claimed the DMA 220 updates (*updating some of the registers...*) the registers 340 in response to a zone transition event. (see specification, for example, pg. 3 lines 1-10; pg. 5 lines 5-12; pg. 8 lines 15-16). The data transfers (*retrieving a first portion of the recorded data...retrieving a second portion of the recorded data...*) are controlled by the microcontroller 210. Like Liu '617, the DMA 220 updates transient state information in response to initiation of a data transfer command by the top level microcontroller 210. Unlike Liu '617, however, both the DMA 220 and the microcontroller 210 transact over the common bus 360 (*via the bus...*)

Accordingly, the Examiner's claim construction is unreasonably broad because it ignores the plain meaning known to the skilled artisan as well as the explicit definition from both the specification and the cited reference of the claim phrase *updating some of the registers via the bus*. *In re Morris*, 43 USPQ2d 1753 (Fed. Cir. 1997). The Examiner's basis for this rejection is erroneous because it relies on a mischaracterization of Liu '617. Absent the mischaracterization, Liu '617 cannot sustain a Section 102 rejection because it does not identically disclose all the features of the present invention as claimed.

Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the finality of this anticipatory rejection of claim 1 and the claims depending therefrom. Otherwise, this case is not in condition for appeal because of the unresolved issue that the rejection is clearly not proper and without basis due to the legal deficiency associated with the Examiner's mischaracterization of the cited reference. Basing anticipation on a mischaracterization of the cited reference violates the Examiner's obligation of completeness in considering the patentability of the present invention as claimed. 37 CFR 1.104(a) This case is also not in condition for appeal due to the unresolved issue that, absent the mischaracterization, the rejection is clearly not proper and without basis because the Examiner has failed to cite a reference that identically discloses all the recited features of the rejected claims, thereby failing to substantiate a prima facie case of anticipation.

Claim 16

The Examiner has not substantiated the requisite prima facie case of anticipation because Liu '617 does not identically disclose all the features of the present embodiments according to claim 16, which include at least the following:

> *A method comprising steps of: (a) providing data via a bus; (b) updating at least one register or parameter via the bus; and (c) providing data via the bus responsive to the updating.*
> (claim 16, emphasis added)

As above for claim 1, Applicant previously argued that Liu '617 clearly does not disclose *updating at least one register...via the bus* as in the present embodiments as claimed. (Applicant's response of 8/10/2005, pg. 6) The Examiner maintained the

rejection on the same basis as before, and bolstered it by the mischaracterization that Liu '617 discloses the host 210 updating the registers 320.

Accordingly, as above for claim 1 the Examiner's claim construction is unreasonably broad because it ignores the plain meaning known to the skilled artisan as well as the explicit definition in both the present specification and the cited reference for the claimed feature *updating at least one register or parameter via the bus*.... *In re Morris*, 43 USPQ2d 1753 (Fed. Cir. 1997). The Examiner's basis for this rejection is erroneous because it relies on a mischaracterization of Liu '617. Absent the mischaracterization, Liu '617 cannot sustain a Section 102 rejection because it does not identically disclose all the features of the present invention as claimed.

Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the finality of this anticipatory rejection of claim 16 and the claims depending therefrom. Otherwise, this case is not in condition for appeal because of the unresolved issue that the rejection is clearly not proper and without basis due to the legal deficiency associated with the Examiner's mischaracterization of the cited reference. Basing anticipation on a mischaracterization of the cited reference violates the Examiner's obligation of completeness in considering the patentability of the present invention as claimed. 37 CFR 1.104(a) This case is also not in condition for appeal due to the unresolved issue that, absent the mischaracterization, the rejection is clearly not proper and without basis because the Examiner has failed to cite a reference that identically discloses all the recited features of the rejected claims, thereby failing to substantiate a prima facie case of anticipation.

Rejection Under Section 103(a)

Claims 2-5 were rejected as being unpatentable over Liu '617 in view of Cloke '452. Applicant respectfully traverses this rejection because these claims in the least are allowable as depending from an allowable independent claim, for reasons above, and providing additional limitations thereto.

Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the finality of this rejection of claims 2-5. Otherwise, this case is not in condition for appeal because of the unresolved issues that the rejection is clearly not proper and without basis due to the legal deficiencies and lack of a substantiated prima facie case of anticipation discussed above.

Rejection Under Section 103(a)

Claims 15 and 20 were rejected as being unpatentable over Liu '617 in view of Bowes '856. Applicant respectfully traverses this rejection.

Claim 15

The Examiner has not substantiated a prima facie case of obviousness, at least because Liu '617 in view of Bowes '856 do not disclose or suggest all the features of the present invention as claimed which include at least the following:

> *An apparatus comprising...a memory containing several values indexed by zone identifiers; a first controller chip containing a microprocessor and a direct memory access (DMA) controller, the DMA controller operatively coupled to the memory; a first channel chip having several registers; and a bus operatively coupled between the interface and the chips, the bus controllable by the DMA*

> *controller to read from the memory and to update several of the registers in response to a zone transition event.*
> (excerpt of claim 15, emphasis added)

First, Liu '617 is wholly silent regarding *a memory containing several values indexed by zone identifiers*. In fact, Liu '617 is wholly silent regarding zone-based data storage, not even employing the term "zone" whatsoever. The passage of Liu '617 on which the Examiner relies (col. 13 lines 21-28) has absolutely nothing to do with storing values in a memory that are indexed by zone identifiers. Rather, that passage discloses an initialization routine whereby during a power-on reset the auto-write sector counter is set to a value associated with the allocation of memory in RAM 222 by the microprocessor 221. It is very curious to Applicant why the Examiner provides no other basis than this unrelated passage for the assertion that Liu '617 discloses a memory with information that is indexed by zone identifiers. Absent any explanation, Applicant can only conclude that the Examiner has mischaracterized Liu '617, and has requested a telephone interview to clarify this factual issue.

Bowes '856 does not cure the deficient teaching of Liu '617 in this regard, being likewise wholly silent regarding zone-based recording, and likewise not even employing the term "zone" whatsoever. Note also the related issue that these references do not, neither alone nor combined, disclose or suggest updating the registers in response to a *zone transition event* as in the present embodiments as claimed. Accordingly, the Examiner has failed to substantiate a prima facie case of obviousness because the cited references do not, neither alone nor in combination, disclose or suggest these features of the present embodiments as claimed.

Second, Liu '617 is wholly silent regarding *the bus controllable by the DMA controller to...update several of the registers*. The Examiner reads the recited *bus* onto the host bus 215 of Liu '617. However, as discussed above in detail for claim 1, Liu '617 does not disclose or suggest updating the registers 320 over the bus 215. Bowes '856 does not cure the deficient teaching of Liu '617 in this regard. Accordingly, the Examiner has also failed to substantiate a prima facie case of obviousness because the cited references do not, neither alone nor in combination, disclose or suggest this feature of the present embodiments as claimed.

Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the finality of this obviousness rejection of claim 15. Otherwise, this case is not in condition for appeal because of the unresolved issue that the rejection is clearly not proper and without basis due to the Examiner's failure to cite references that, either alone or combined, disclose(s) all the recited features of the rejected claims, thereby failing to substantiate the requisite prima facie case of obviousness.

Claim 20

Applicant respectfully traverses this rejection because this claim in the least is allowable as depending from an allowable independent claim, for reasons above, and providing additional limitations thereto.

Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the finality of this rejection of claim 20. Otherwise, this case is not in condition for appeal because of the unresolved issues that the rejection is clearly not proper and

without basis due to the legal deficiencies and lack of a substantiated prima facie case of obviousness discussed above.

Rejection Under 35 USC 103(a)

Claims 6-14 were rejected as being unpatentable over Liu '617 in view of Cloke '452 and further in view of Bowes '856. Applicant respectfully traverses this rejection.

Claim 6

The Examiner has not substantiated the requisite prima facie case of obviousness because Liu '617 in view of Cloke '452 and further in view of Bowes '856 do not, neither alone nor in combination, disclose or suggest all the features of the present invention as claimed which include at least the following:

> *retrieving via the DMA controller several values indexed by zone identifier* Z_B*...updating at least some of the read channel register values from the retrieved values....*
> (excerpt of claim 6, emphasis added)

First, as above Applicant expressly traverses the Examiner's assertion that Liu '617's RAM 222 and the cited passage (col. 13 lines 21-28) disclose the *value table indexed by a zone identifier* as recited in the preamble of claim 6. Support for the recited *value table* is found at least in the memory table 230 of FIG. 2 wherein blocks of values 229, such as head bias 251, gain 252, sectors/track 253 and the like, are indexed according to zone identification references 228. As discussed above, absent a

clarification from the Examiner, the Applicant can only conclude that the Examiner has again mischaracterized the disclosure of Liu '617.

Furthermore, Applicant expressly traverses the Examiner's assertion that Liu '617 in the cited passage (col. 7 line 37 to col. 8 line 33) discloses *retrieving via the DMA controller several values indexed by zone identifier* as in the present embodiments as claimed. This cited passage generally discloses how the bus interface circuit 234 in Liu '617 transfers data to and from the RAM 222 during execution of a data transfer command without intervention by the microprocessor 221, thereby reducing the overhead on the host bus 215. The only reference to the RAM 222 in this passage, which Examiner views as anticipating the *value table* of the present embodiments, does not disclose retrieving values indexed therein by a zone identifier:

> Since automatic read sequencer 250 and automatic write sequencer 260 within computer bus interface circuit 234 transfer multiple sectors of data to (a write operation) and from (a read operation) buffer RAM 222 without intervention by microprocessor 221, sequencers 250, 260 significantly reduce the time required to transfer data between computer 210 and disk drive 220 in comparison to prior art disk drive 120 described above.
> (Liu '617 col. 7 lines 53-60, emphasis added)

Furthermore, Applicant expressly traverses any implication that the Examiner's comment that "note the zone is denoted using the cylinder and sector address" meaningfully cures the irrelevance of the cited passage. Basically, as discussed above, Liu '617 is wholly silent regarding zone-based recording, and so the Examiner's extrapolation that the zone is denoted in any way can again only be concluded as the Examiner's mischaracterization of what Liu '617 actually discloses.

Furthermore, because Liu '617 discloses neither the *value table indexed by zone identifiers* nor *retrieving...several values indexed by zone identifier*, Applicant expressly traverses the Examiner's assertion that Liu '617 in the cited passage (col. 8 lines 34-39, lines 64-67) discloses *updating at least some of the read channel register values from the retrieved values* as in the present embodiments as claimed. These cited passages generally disclose how in Liu '617 the read sequencer 250 and write sequencer 260, respectively, of the bus interface circuit 234 update the transient state information, such as head number, cylinder address, sector address, and the number of sectors remaining to be transferred in task file registers. This passage, and Liu '617 as a whole, is silent regarding updating the register with the retrieved values that are indexed by zone identifier as in the present embodiments as claimed.

Furthermore, as discussed above neither Cloke '452 nor Bowes '856 cure the deficiencies of Liu '617 in these regards. Accordingly, the Examiner has failed to substantiate a prima facie case of obviousness because the cited references do not, neither alone nor in combination, disclose or suggest this feature of the present embodiments as claimed.

Furthermore, even if the cited references did disclose or suggest all the features of the rejected claims, which they do not as discussed above, the Examiner provides no substantiated basis for express motivation to combine and/or modify the cited references to arrive at the present embodiments as claimed. In the absence of express motivation to combine the references, a statement that modifications of the prior art to meet the claimed invention would have been within the knowledge of a skilled artisan because all aspects of the claimed invention are individually taught by different references is not sufficient to

substantiate the motivation or suggestion required by a bona fide prima facie case of obviousness. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993); *In re Kotzab*, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000); *Al-Site Corp. v. VSI Int'l Inc.*, 50 USDPQ2d 1161 (Fed. Cir. 1999); MPEP 2143.01.

Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the finality of this obviousness rejection of claim 6 and the claims depending therefrom. Otherwise, this case is not in condition for appeal because of the unresolved issue that the rejection is clearly not proper and without basis due to the Examiner's failure to cite references that, either alone or combined, disclose(s) all the recited features of the rejected claims, thereby failing to substantiate the requisite prima facie case of obviousness. This case is also not in condition for appeal because of the unresolved issue that the rejection is clearly not proper and without basis due to the Examiner's failure to substantiate a motivation to modify and/or combine the references to arrive at the present invention as claimed, thereby failing to substantiate the requisite prima facie case of obviousness.

Conclusion

This is a complete response to the pending Office Action of 10/25/2005.

Applicant has also filed herewith a Request for Telephone Interview to be held before the Examiner makes the next action on the merits. The interview is necessary, absent allowance, to settle the unresolved issues making this case presently not in condition for appeal.

Should any questions arise concerning this application, the Examiner is encouraged to contact the below signed attorney.

Respectfully submitted,

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